

**KAF- 3200E  
KAF- 3200ME**

**2184 (H) x 1472 (V) Pixel**

**Full-Frame CCD Image Sensor**

**Performance Specification**

**Eastman Kodak Company**

**Image Sensor Solutions**

**Rochester, New York 14650-2010**

**Revision 1**

**September 26, 2001**

**Eastman Kodak Company – Image Sensor Solutions**

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# KAF-3200E / KAF-3200ME

## 1.1 Features

- **3.2 Million Pixel Area CCD**
- **2184 H x 1472V Pixels**
- **Transparent Gate True Two Phase Technology with and without micro lens (Enhanced Spectral Response)**
- **6.8 x 6.8 $\mu$ m Pixels**
- **14.85mm H x 10.26mm V Photosensitive Area**
- **100% Fill Factor**
- **High Output Sensitivity (20 $\mu$ V/e-)**
- **78 dB Dynamic Range**
- **Low Dark Current (<7pA/cm<sup>2</sup> @ 25°C)**

## 1.2 Description

The KAF-3200E is a high performance monochrome area CCD (charge-coupled device) image sensor with 2184H x 1472V photoactive pixels designed for a wide range of image sensing applications in the 0.3nm to 1.0nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 75dB dynamic range is possible operating at room temperature.

The sensor is built with a true two-phase CCD technology employing a transparent gate and with micro lenses available. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard poly silicon gate technology. The micro lenses are an integral part of each pixel and cause most of the light to pass through the transparent gate half of the pixel, further improving the spectral sensitivity.

The photoactive area is 14.85mm x 10.26mm and is housed in a 24 pin dual in line (DIP) package with 0.1" pin spacing.

The sensor consists of 2254 parallel (vertical) CCD shift registers each 1510 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 2267 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

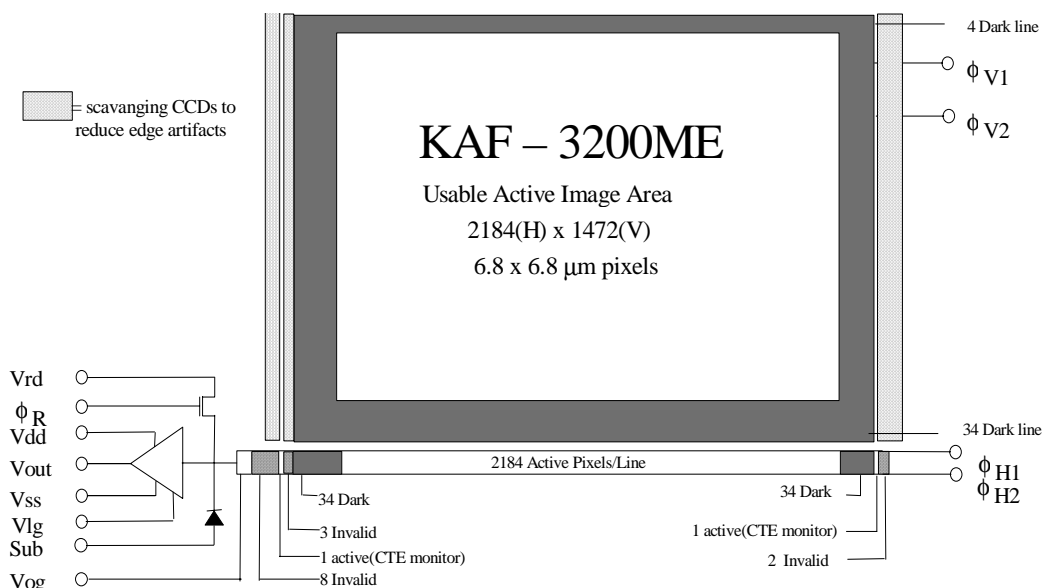


Figure 1 – Block Diagram

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## 1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the  $\Phi V1$  and  $\Phi V2$  register clocks are held at a constant (low) level.

See Figure 5. - Timing Diagrams.

## 1.4 Charge Transport

Referring again to Fig.-ure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the  $\Phi V1$  and  $\Phi V2$  register clocks. The horizontal CCD is presented a new line on the falling edge of  $\Phi V1$  while  $\Phi H2$  is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the  $\Phi H1$  and  $\Phi H2$  pins in a complementary fashion. On each falling edge of  $\Phi H1$  a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

## 1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate ( $\Phi R$ ) is clocked to remove the signal and FD is reset to the potential applied by VRD. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4.

## 1.6 Dark Reference Pixels

At the beginning of each line are 34 light shielded pixels. There is also 34 full dark line at the start of every frame and 4 full dark line at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, (including the 2 full dark lines and one column at end of each line), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

## 1.7 Transfer Efficiency Test Pixels and Dummy Pixels

At the beginning of each line and at the end of each line are extra horizontal CCD pixels. These are a combination of pixels that are not associated with any vertical CCD register and two that are associated with extra photoactive vertical CCDs. These are provided to give an accurate photosensitive signal that can be used to monitor the charge transfer efficiency in the serial (horizontal) register.

They are arranged as follows beginning with the first pixel in each line

- 8 dark, inactive pixels
- 1 photoactive
- 3 inactive pixels
- 34 dark reference pixels
- 2184 photoactive pixels
- 34 dark pixels
- 1 photo active pixel
- 1 inactive pixels

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# KAF-3200E / KAF-3200ME

## 2.1 Package Drawing

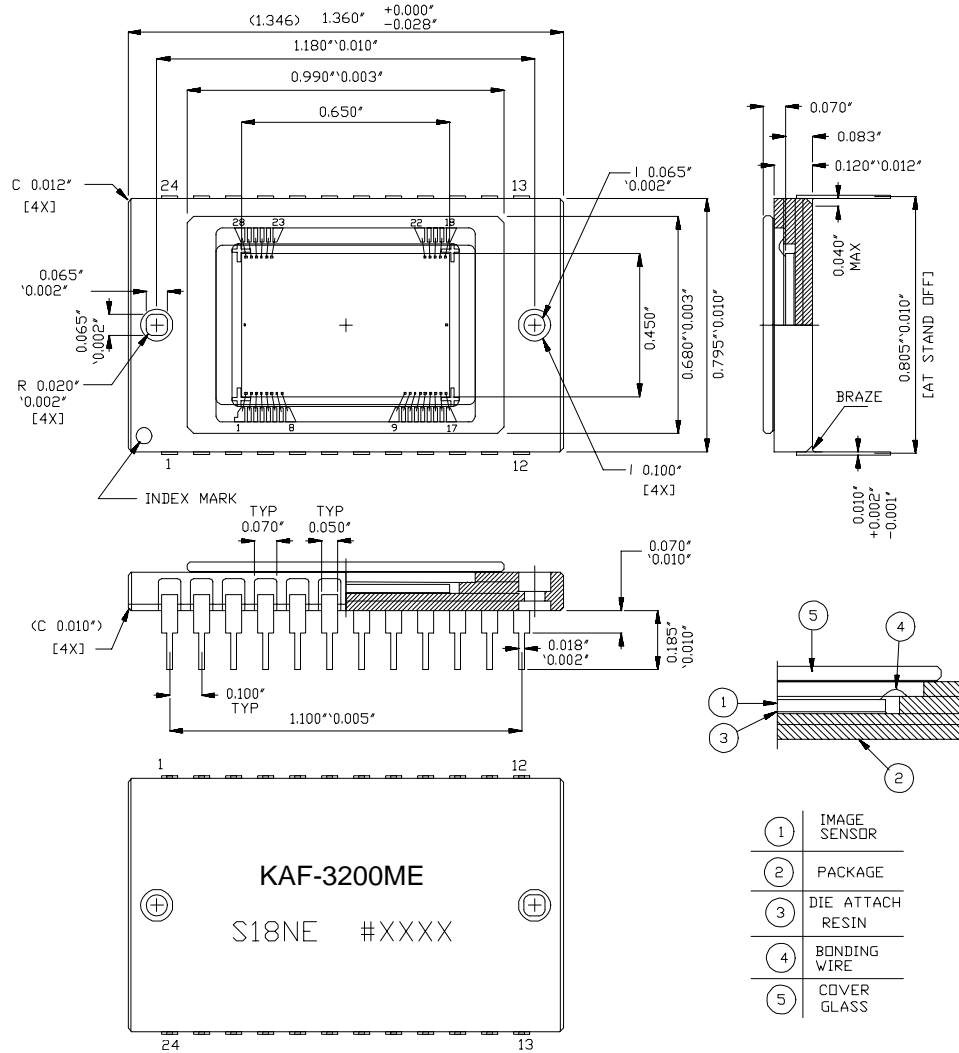


Figure 2 - Package Drawing

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## 2.2 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	VOG	Output Gate	12, 13, 14	VSUB	Substrate (Ground)
2	VOUT	Video Output	15, 16, 21, 22	$\phi V_1$	Vertical CCD Clock - Phase 1
3	VDD	Amplifier Supply	17, 18, 19, 20	$\phi V_2$	Vertical CCD Clock - Phase 2
4	VRD	Reset Drain	23	VGuard	Guard Ring
5	$\phi R$	Reset Clock	24	N/C	No Connection (open pin)
6	VSS	Amplifier Supply Return			
7	$\phi H_1$	Horizontal CCD Clock - Phase 1			
8	$\phi H_2$	Horizontal CCD Clock - Phase 2			
9, 10, 11	N/C	No connection (open pin)			

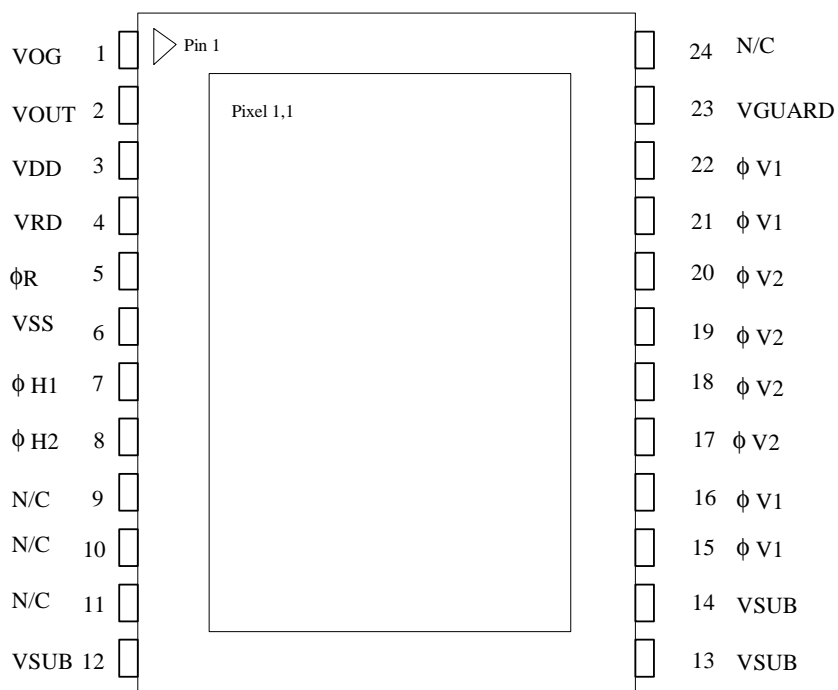


Figure 3 - Package Pin Assignments

**Note:**

The KAF-3200E is designed to be compatible with the KAF-1602 and KAF-0401 series of Image sensors. The exception is the addition of two new Vsub connections on pins 12 and 13.

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## 3.1 Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1, 2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1, 3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1, 4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Storage Temperature	T		100	°C	
Humidity	RH	5	90	%	7

**Notes:**

1. Referenced to pin Vsub.
2. Includes pins: VRD, Vdd, Vss, Vout.
3. Includes pins:  $\phi V1$ ,  $\phi V2$ ,  $\phi H1$ ,  $\phi H2$ .
4. Includes pins: Vog, Vlg.,  $\phi R$
5. Voltage difference between overlapping gates. Includes:  $\phi V1$  to  $\phi V2$ ,  $\phi H1$  to  $\phi H2$ ,  $\phi V2$  to  $\phi H1$ ,  $\phi H2$  to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T=25°C. Excessive humidity will degrade MTTF.

**CAUTION:** This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance to strict ESD procedures for Class 0 (HBM) devices.

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## 3.2 DC Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Max DC Current (mA)	Notes
Reset Drain	VRD	11	12	12.25	V	0.01	
Output Amplifier Return	VSS	2.5	3.0	3.2	V	-0.5	
Output Amplifier Supply	VDD	14.5	15	15.25	V	Iout	
Substrate	VSUB	0	0	0	V	0.01	
Output Gate	VOG	4.75	5	5.5	V	0.01	
Guard	VGUARD	9	10	12	V		
Video Output Current	Iout		-5	-10	mA	-	1

**Notes:**

1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

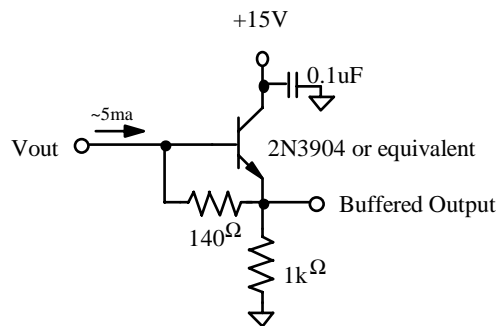


Figure 4 – Typical Output Structure Load Diagram  
For operation of up to 10 MHz\

The value of R1 depends on the desired output current according the following formula:  $R1 = 0.7 / I_{out}$

The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5mA is recommended for capacitance of 12pF and pixel rates up to 15MHz.

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### 3.3 AC Operating Condition

Description	Symbol	Level	Min.	Nom.	Max.	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	$\phi V1$	Low	-10.0	-8.5	-8.5	V	50 nF (all $\phi V1$ pins)
		High	0.0	2.0	3.0	V	
Vertical CCD Clock - Phase 2	$\phi V2$	Low	-10.0	-8.5	-8.5	V	50 nF (all $\phi V2$ pins)
		High	0.0	2.0	3.0	V	
Horizontal CCD Clock - Phase 1	$\phi H1$	Low	-3.5	-3.0	-2	V	150 pF
		High	$\phi H1$ Low + 10	7.0	$\phi H1$ Low + 10	V	
Horizontal CCD Clock - Phase 2	$\phi H2$	Low	-3.5	-3.0	-2	V	150 pF
		High	$\phi H1$ Low + 10	7.0	$\phi H1$ Low + 10	V	
Reset Clock	$\phi R$	Low	3.0	4.0	4.25	V	5pF
		High	10.0	11.0	11.25	V	

**Notes:**

1. All pins draw less than 10uA DC current.

### 3.4 AC Timing Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
$\phi H1, \phi H2$ Clock Frequency	$f_H$		10	12	MHz	1, 2, 3
Pixel Period	$t_e$	67	100		ns	
$\phi H1, \phi H2$ Setup Time	$t_{\phi HS}$	0.5	1		us	
$\phi V1, \phi V2$ Clock Pulse Width	$t_{\phi V}$	4	5		us	2
Reset Clock Pulse Width	$t_{\phi R}$	5	20		ns	4
Readout Time	$t_{readout}$	252.5	366.3		ms	5
Integration Time	$t_{int}$					6
Line Time	$t_{line}$	167.2	242.6		us	7

**Notes:**

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4.  $\phi R$  should be clocked continuously.
5.  $t_{readout} = (1510 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark field pattern and shot noise.
7.  $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + (2267 * t_e) + t_e$

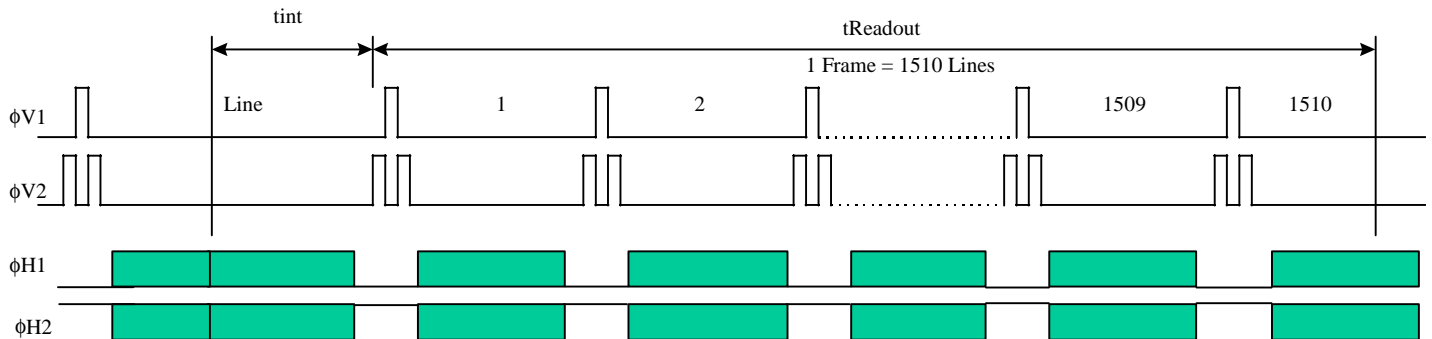
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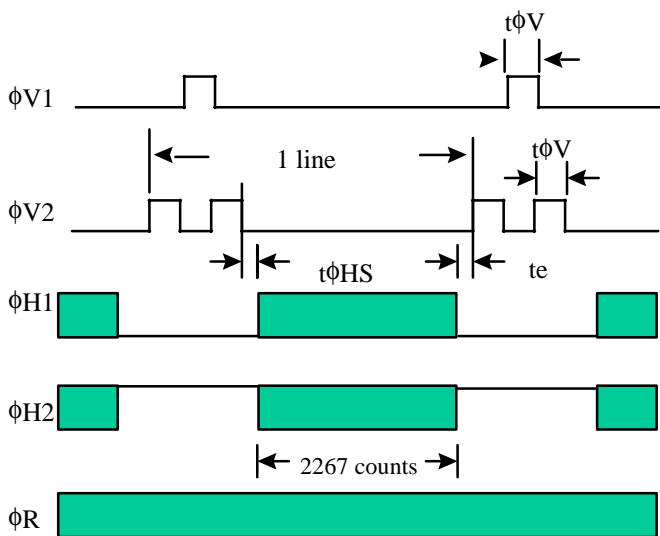
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## 3.5 Clock Timing

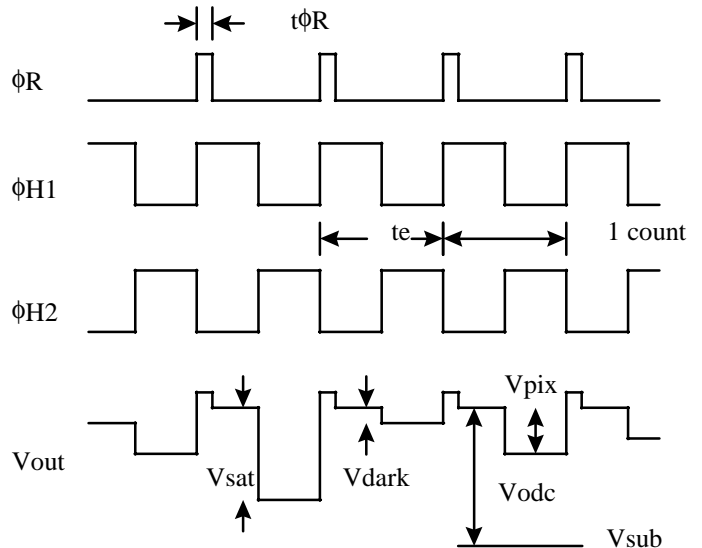
### Frame Timing



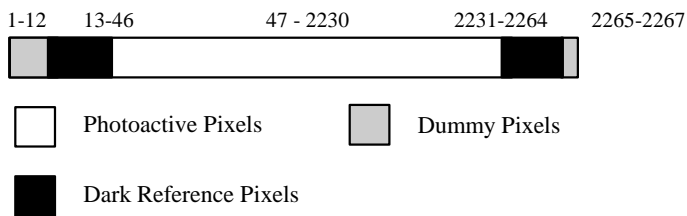
### Line Timing Detail



### Pixel Timing Detail



### Line Content



$V_{sat}$  Saturated pixel video output signal  
 $V_{dark}$  Video output signal in no light situation, not zero due to  $J_{dark}$   
 $V_{pix}$  Pixel video output signal level, more electrons = more negative  
 $V_{dc}$  Video level offset with respect to  $V_{sub}$   
 $V_{sub}$  Analog Ground

\* See Image Acquisition section (page 4)

Figure 5 - Timing Diagrams

Note :

The KAF-3200E was designed to be compatible with the KAF-1602 and KAF-0401 series of image sensors. Please note that the polarities of the two-phase clocks have been swapped on the KAF-3200E compared to the KAF-1602 and KAF-0401.

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## 4.1 Performance Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	50000 100000 100000	55000 110000 110000	120000	electrons / pixel	1
Red Quantum Efficiency ( $\lambda=650\text{nm}$ )	Rr	60	65	70	%	
Green Quantum Efficiency ( $\lambda=550\text{nm}$ )	Rg	46	52	57	%	
Blue Quantum Efficiency ( $\lambda=450\text{nm}$ )	Rb	32	40	44	%	
Blue Quantum Efficiency ( $\lambda=400\text{nm}$ )	Rb(400)	28	32	37	%	
Photoresponse Non-Linearity	PRNL		1	2	%	2
Photoresponse Non-Uniformity	PRNU		1	3	%	3
Dark Signal	Jdark		15 6	30 10	electrons / pixel / sec pA/cm <sup>2</sup>	4 25 C
Dark Signal Doubling Temperature		5	6	7	°C	
Dark Signal Non-Uniformity	DSNU		15	30	electrons / pixel / sec	5
Dynamic Range	DR	72	77		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99999			
Output Amplifier DC Offset	V <sub>odc</sub>	VRD - 2	VRD - 1	VRD	V	7
Output Amplifier Bandwidth	f <sub>-3dB</sub>		45		Mhz	8
Output Amplifier Sensitivity	V <sub>out</sub> /N <sub>e~</sub>	18	20		uV/e~	
Output Amplifier output Impedance	Z <sub>out</sub>	175	200	250	Ohms	
Noise Floor	ne~		7	12	electrons	9

### Notes:

- For pixel binning applications, electron capacity up to 150,000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
- Worst-case deviation from straight line fit, between 2% and 90% of Nsat.
- One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
- Average of all pixels with no illumination at 25°C.
- Average dark signal of any of 11 x 8 blocks within the sensor. (each block is 128 x 128 pixels)
- $20\log(Nsat / ne~)$  at nominal operating frequency and 25°C.
- Video level offset with respect to ground
- Last output amplifier stage only. Assumes 10pF off-chip load..
- Output noise at -10°C, 1MHz operating frequency (15MHz bandwidth), and tint = 0 (excluding dark signal).

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## 4.2 Typical Performance Characteristics

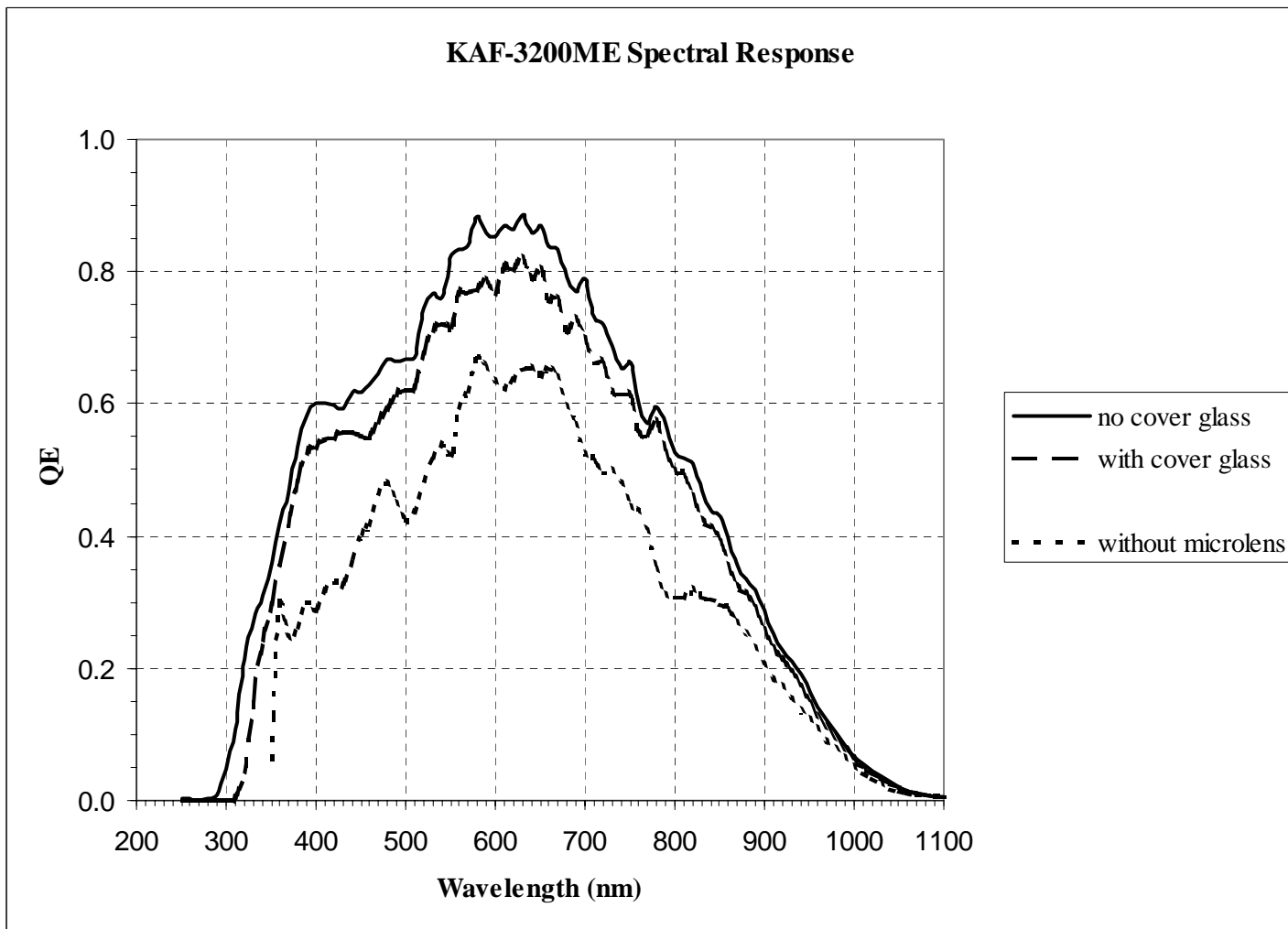


Figure 6 – Spectral Response

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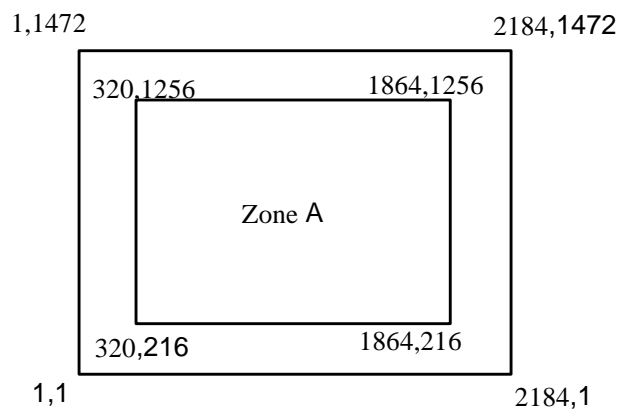
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## 4.3 Cosmetic Classification

Defect tests performed at T=25°C

Class	Point Defects		Cluster Defects		Column	
	Total	Zone A	Total	Zone A	Total	Zone A
C1	≤5	≤2	0	0	0	0
C2	≤10	≤5	≤4	≤2	0	0



Zone A = Central 1544H x 1040V Region

Point Defect	DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR BRIGHT: A Pixel with dark current > 5000 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects
Column Defect	1) A grouping of >5 contiguous point defects along a single column, 2) A column containing a pixel with dark current > 12,000e/pixel/sec (bright column) 3) A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column) 4) A column which loses more than 250 e under 2Ke illumination.(trap defect))
Neighboring pixels Defect Separation	The surrounding 128 x 128 pixels or ±64 columns/rows. Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

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## 5.1 Quality Assurance and Reliability

- 5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.
- 5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.
- 5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.
- 5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe workstations.
- 5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.
- 5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

## 5.2 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions  
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Rochester, New York 14650-2010  
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### **WARNING: LIFE SUPPORT APPLICATIONS POLICY**

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

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## Changes:

Revision Number	Changes
0	Originally KAF-3200E, Revision No. 0.
1	Microlens version added. Updated V clock voltages, replaced spectral response with micro lens version. Added description of micro lens enhanced response. Removed grades 0 and 3.

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